Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently Amended) A method of generating digital traffic for use in testing a multi-port communication device, said method comprising the steps of:

generating a reference digital traffic pattern;

generating a plurality of traffic streams replicated from the reference digital traffic pattern, wherein the plurality of traffic streams are used for loading respective input ports of the communication device; and

introducing a plurality of phase delays among the plurality of traffic streams when compared to the reference digital traffic pattern, such that transmission of one traffic stream of said plurality of traffic streams has a phase delay determined from a length of a buffer associated with said one traffic stream and ~~traffic streams~~ begins at a time between boundaries of time units of a transmission rate associated with said one traffic stream.

Claim 2. (Cancelled)

Claim 3. (Previously Presented) The method according to claim 48 wherein the communication device effects statistical multiplexing amongst the plurality of traffic streams.

Claim 4. (Previously Presented) The method according to claim 3, wherein the plurality of traffic streams are continuous digital data streams.

Claim 5. (Previously Presented) The method according to claim 4, wherein the plurality of traffic streams are ATM cell streams.

Claim 6. (Previously Presented) A method of loading a multi-port communication device with digital traffic, the method comprising the steps of:

generating a digital traffic pattern; and

providing a plurality of streams replicated from the digital traffic pattern to input ports of the communication device, the plurality of streams having a plurality of phase delays therebetween, such that transmission of at least one stream of said plurality of streams begins at a time between boundaries of time units of a transmission rate associated with said each of said digital traffic pattern and has a phase delay determined by at least a length of a buffer associated with said at least one stream.

Claim 7. (Previously Presented) The method according to claim 6, wherein the communication device effects statistical multiplexing of the plurality of streams.

Claim 8. (Previously Presented) A method of loading a multi-port communication device with digital traffic, said method comprising the steps of:

generating from a digital traffic stream with a plurality of digital traffic streams having identical data content thereto; and

providing the plurality of digital traffic streams with a plurality of phase delays therebetween to input ports of the communication device, each phase delay being related to a buffer length, such that the phase delay is determined from a ratio utilizing the length of said buffer associated with at least one of said plurality of traffic streams, wherein transmission of at least one of said plurality of digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with said each of said digital traffic.

Claim 9. (Previously Presented) The method according to claim 8, wherein the communication device effects statistical multiplexing of the plurality of digital traffic streams.

Claim 10. (Currently Amended) A method of operating a digital traffic replicating device for use in testing a multi-port communication device, comprising the steps of:

receiving an input digital traffic stream; and

generating a plurality of output digital traffic streams from the input digital traffic stream, wherein

a phase delay is introduced to at least one stream of the plurality of output digital traffic streams [[,]] ;

said phase delay is determined from a ratio utilizing a buffer length associated with at least one stream; transmission of said at least one of the plurality of output digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with said input digital traffic stream ; [[,]] and ~~wherein~~

the plurality of output digital traffic streams have traffic patterns which are replicas of the input digital traffic stream.

Claim 11. (Cancelled)

Claim 12. (Previously Presented) The method according to claim 10, wherein the

communication device effects statistical multiplexing of the plurality of output digital traffic streams.

Claim 13. (Previously Presented) An apparatus for generating digital traffic for use in testing a multi-port communication device, said apparatus comprising:

a reference pattern generator generating a reference pattern defining a digital traffic pattern;

a traffic stream replicating device generating a plurality of traffic streams replicated from the reference pattern; and

a phase delay module providing respective phase delays among the plurality of traffic streams utilizing a series of buffers, such that transmission of at least one traffic stream of said plurality of traffic streams is provided with a phase delay based on a length of a buffer of said buffers associated with said at least one traffic stream and begins at a time between boundaries of time units of a transmission rate associated with said plurality of traffic streams,

wherein the plurality of traffic streams load respective input ports of the communication device.

Claim 14. (Cancelled)

Claim 15. (Previously Presented) The apparatus according to claim 49, wherein the communication device effects statistical multiplexing of the plurality of traffic streams.

Claim 16. (Previously Presented) The apparatus according to claim 15, wherein the plurality of traffic streams are continuous digital data streams.

Claim 17. (Previously Presented) The apparatus according to claim 16, wherein the plurality of traffic streams are ATM cell streams.

Claim 18. (Currently Amended) An apparatus for loading a multi-port communication device with digital traffic, the apparatus comprising:

a traffic generator generating input digital traffic; and

a traffic manager providing a plurality of streams replicated from the input digital traffic to input ports of the communication device, one stream of the plurality of streams having a phase delay being determined from a length of a buffer associated with said one stream such that transmission of said one stream begins at a time between boundaries of time units of a transmission rate associated with said input digital stream.

Claim 19. (Previously Presented) The apparatus according to claim 18, wherein the communication device effects statistical multiplexing of the plurality of streams and said phase delay is determined from a ratio utilizing said length of said buffer associated with said each stream and said transmission rate.

Claim 20. (Previously Presented) Apparatus for loading a multi-port communication device with digital traffic, the apparatus comprising:

a traffic generating module generating from a digital traffic stream a plurality of digital traffic streams having identical data content thereto; and

a traffic manager providing the plurality of digital traffic streams to input ports of the communication device with a phase delay introduced to at least one of the plurality of digital traffic streams being determined from a buffer length and a transmission rate associated with said at least one of the plurality of digital traffic streams such that transmission of said at least one of the plurality of digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with said input digital traffic.

Claim 21. (Previously Presented) The apparatus according to claim 20, wherein the communication device effects statistical multiplexing of the plurality of digital traffic streams.

Claim 22. (Currently Amended) A digital data stream replicating device, comprising:

an input port for receiving an input continuous digital data stream comprising input data blocks at an input transmission rate;

a traffic replicator to replicate the input continuous digital data stream into N streams of replicated continuous digital data streams;

N output ports for transmitting the plurality of replicated continuous digital data streams at output transmission rates, each output transmission rate at least equal to the input transmission rate; and

a delay module providing a predetermined delay for each replicated continuous digital data stream of the plurality of replicated digital data streams with respect to the input continuous digital data stream, such that transmission of at least one stream of said each replicated continuous digital data stream has a phase delay determined from a length of a buffer associated with at least one stream and begins at a time between boundaries of time units of a transmission rate associated with said input digital traffic.

Claim 23. (Previously Presented) The device according to claim 22, the device further including an idle block generator for introducing idle data blocks into a replicated continuous digital data stream of the plurality of replicated continuous digital data streams for transmission through an output port of the N output ports when an output

transmission rate associated with the output port is greater than the input transmission rate.

Claim 24. (Previously Presented) The device according to claim 22, wherein the delay module comprises:

a memory having N first-in first-out (FIFO) logical buffers established therein, each logical buffer being associated with one digital data stream of the plurality of replicated continuous digital data streams,

wherein when a logical buffer of the N FIFO logical buffers is full, data blocks associated with the logical buffer are forwarded to an output port of the N output ports associated with the logical buffer.

Claim 25. (Previously Presented) The device according to claim 23, wherein the delay module comprises:

a memory having N first-in first-out (FIFO) logical buffers established therein, each logical buffer being associated with one digital data stream of the plurality of replicated continuous digital data streams,

wherein when a logical buffer of the N FIFO logical buffers is full, data blocks associated with the logical buffer are forwarded to an output port of the N output ports associated

the logical buffer, such that said delay provided to a digital data stream transmitted through the output port correlates to a length of the logical buffer and its associated transmission rate.

Claim 26. (Previously Presented) The device according to claim 25, wherein:

the delay module for each replicated continuous output digital data stream forwards data blocks associated with its logical buffer at the output transmission rate of the corresponding output port; and

the delay provided to the replicated continuous digital data stream correlates to a transmission rate of the corresponding output port.

Claim 27. (Previously Presented) The device according to claim 24, wherein each of the logical buffers is established by copying the input data blocks into a physical buffer organized in the memory, each of the logical buffers corresponding to a different physical buffer.

Claim 28. (Previously Presented) The device according to claim 26, each of the logical buffers is established by copying the input data blocks into a physical buffer organized in the memory, each of the logical buffers corresponding to a different physical buffer.

Claim 29. (Previously Presented) The device according to claim 24, wherein the logical buffers are established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

Claim 30. (Previously Presented) The device according to claim 26, wherein the logical buffers are established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

Claim 31. (Previously Presented) The device according to claim 24, wherein the input and transmitted digital data streams are ATM cell streams.

Claim 32. (Previously Presented) The device according to claim 26, wherein the input and transmitted digital data streams are ATM cell streams.

Claim 33. (Currently Amended) A digital data stream replicating device for providing data traffic input patterns to a communication device, comprising:

an input port for receiving a continuous digital data stream comprising input data blocks at an input transmission rate;

a memory;

N output ports, each having an output transmission rate at least equal to the input transmission rate;

a traffic processor [[,]] connected between the input port and the N output ports, providing N first-in first-out logical buffers in the memory and associating each of the input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and

a scheduler to forward data blocks associated with a given logical buffer through its corresponding output port when the given logical buffer is full, such that transmission of said data blocks begins at a time between boundaries of time units of a transmission rate associated with said corresponding output port and a phase delay associated with said transmission of said data block is determined from at least a length of said logical buffer.

Claim 34. (Previously Presented) The device according to claim 33, wherein each logical buffer has a length selected to achieve a relative delay between the input digital data stream and an output digital data stream replicated by the logical buffer for its corresponding output port.

Claim 35. (Previously Presented) The device according to claim 34, wherein each of the logical buffers is established by copying the input data blocks into a physical buffer

organized in the memory, each of the logical buffers corresponding to a different physical buffer.

Claim 36. (Previously Presented) The device according to claim 34, wherein the logical buffers are established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

Claim 37. (Previously Presented) The device according to claim 34, wherein the input and output digital data streams are ATM streams.

Claim 38. (Cancelled)

Claim 39. (Previously Presented) The device according to claim 33, the device further including an idle traffic generator for introducing empty data blocks into an output digital data stream replicated by the logical buffer for its corresponding output port when the output transmission rate of its corresponding output port is greater than the input transmission rate.

Claim 40. (Previously Presented) The device according to claim 39, wherein, for each logical buffer, its length and the output transmission rate of its corresponding output port are selected to achieve a relative delay between the input digital data stream and an output digital data stream replicated by the logical buffer for its corresponding output port.

Claim 41. (Cancelled)

Claim 42. (Cancelled)

Claim 43. (Previously Presented) The device according to claim 39, wherein the input and output digital data streams are ATM streams.

Claim 44. (Currently Amended) A performance testing device, comprising:

a traffic generator for generating a continuous digital data stream;

an input port for receiving the continuous digital data stream at an input transmission rate;

a broadcaster for replicating the input digital data stream N times;

N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and

a delay module for introducing a predetermined relative delay for each said transmitted digital data stream with respect to the input digital data stream, such that transmission of at least one stream of said each said transmitted digital data stream begins at a time between boundaries of time units of a transmission rate associated with said each transmitted digital data stream and has a phase delay determined by at least a length of a buffer associated with said at least one stream.

Claim 45. (Currently Amended) A performance testing device, comprising:

a traffic generator for generating a continuous digital data stream;

an input port for receiving the continuous digital data stream comprising input data blocks at an input transmission rate;

a memory;

N output ports, each having an output transmission rate at least equal to the input transmission rate;

a traffic processor [[,]] connected between the input port and the N output ports, providing N first-in first-out logical buffers in the memory and associating each of the

input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and

a scheduler for forwarding data blocks associated with a given logical buffer through its corresponding output port when the given logical buffer is full, such that transmission of said data blocks begins at a time between boundaries of time units of an output transmission rate associated with transmission of said data blocks and said transmission has a phase delay determined by at least a length of said logical buffer.

Claim 46. (Previously Presented) The device according to claim 50, the device further including an idle block generator to introduce idle data blocks into an output digital data stream replicated by the logical buffer for its corresponding output port when the output transmission rate of its corresponding output port is greater than the input transmission rate.

Claim 47. (Previously Presented) The method according to claim 1, wherein said phase delay is determined from said length of said buffer and said transmission rate.

Claim 48. (Currently Amended) The method according to claim 47, wherein another traffic stream of said plurality of traffic streams has a second phase delay determined

from a length of a second buffer ~~length~~ associated with said another traffic stream and said transmission rate.

Claim 49. (Previously Presented) The apparatus for generating digital traffic for use in testing a multi-port communication device method as claimed in claim 13, wherein said each phase delay is determined from said length of said buffer and said transmission rate.

Claim 50. (Currently Amended) A performance testing device, comprising:

a traffic generator for generating a continuous digital data stream;

an input port for receiving the continuous digital data stream comprising input data blocks at an input transmission rate;

a memory;

N output ports, each having an output transmission rate at least equal to the input transmission rate;

a traffic processor ~~processing means,~~ connected between the input port and the N output ports, for establishing N first-in first-out logical buffers in the memory and associating each of the input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and

a scheduler ~~scheduling means~~ for forwarding data blocks associated with a given logical buffer through its corresponding output port when the given logical buffer is full, such that transmission of said data blocks begins at a time between boundaries of time

units of an output transmission rate associated with transmission of said data blocks, wherein one of said N first-in first-out logical buffers is a given size and at least another of said N first-in first-out logical buffers is a different size than said given size.